University Côte d'Azur
LEAT Research Lab
UMR CNRS 7248

Research Internship

High-level modeling of Non-Volatile Memories for neuromorphic computing

Context

Hardware neural network implementation is a hot topic in research and is now considered as strategic for several international companies [1]. Leading projects in neuromorphic engineering have led to powerful brain-inspired chips such as SyNAPSE, TrueNorth and SpiNNaker. Most of these technologies work well in centralized computing farms but won't fit embedded systems or Internet-of-Things (IoT) requirements, due to their energy consumption. Heterogeneous integration between CMOS and emergent technologies is seen as an opportunity to go past this limitation. In particular, Magnetoresistive Random-Access Memory (MRAM) is considered one of the most promising Non-Volatile Memory (NVM) technology expected to mitigate energy consumption when integrated in computing architectures. However, we still miss a high-level perspective on how NVM actually benefits energy efficiency and how it can be improved any further [3].

Internship mission

The internship mission will be organized in several periods:

- Theoretical study of NVM-based neuromorphic architectures and scientific bibliography,
- System-level modeling of existing RTL-based neuromorphic accelerators [2],
- Integration of high-level models of Non-Volatile Memory properties,
- Simulation of the SystemC model of the architecture with spiking stimuli coming from an asynchronous camera.

References

[1] *P. Narayanan et al. Toward on-chip acceleration of the backpropagation algorithm using nonvolatile memory. IBM Journal of Research and Development, 61(4):1-11, July 2017.*

[2] V. Lorrain et al. N2D2: a framework for deep neural networks exploration, spike transcoding and code generation for COTS and dedicated HW IPs. In DAC 2017.

[3] *L. Khacef, B. Miramond et al. Hardware implementation of artificial neural networks: From neurosciences to machine learning. Conf. on Parallelism, Architectures and Systems, 2017.*

Practical information

Location : LEAT Lab, Sophia Antipolis and CEA/Spintec, Grenoble
Duration : 6 months from march 2018
Grant : 546 € / month
Profile : Electronics, embedded systems, neural networks, SystemC/C++ progr. language

Contact

Benoît Miramond
LEAT Lab – University Côte d'Azur
benoit.miramond@unice.fr / 04.92.94.28.84
Francois Duhem
CEA/Spintec - Grenoble
francois.duhem@cea.fr / 04.38.78.52.98